

REMARKS:

Applicant appreciates the thorough examination of the present application that is reflected in the Final Official Action of November 13, 2002. Minor changes are made to the specification. Claims 5, 6, 10, 12-20, 25-27 and 30 are cancelled without prejudice or disclaimer. Claims 12-20 have been cancelled in response to the restriction requirement. Claims 1, 21, 28 and 32 are amended; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Applicant believes the foregoing amendments comply with requirements of form and thus may be entered under 37 C.F.R. § 1.116(a) as presenting rejected claims in better form for consideration on appeal. Alternatively, to the extent any of these amendments are deemed to touch the merits, then entry is requested under 37 C.F.R. § 1.116(b). These amendments were not earlier presented because they are in response to the matters pointed out for the first time in the Final Office Action. New claims 33-43 are added. Claims 1-4, 7, 9, 11, 21-24, 28-29 and 31-43 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Claims 1, 21 and 32

Claims 1 and 32 were rejected as being anticipated by Gardner et al. (USPN 6201278). Claim 21 was rejected as being obvious over Gardner et al. (USPN 6201278) in view of Murthy et al. (USPN 6214679).

Claims 1, 21 and 32 have been amended to further distinguish those claims over the cited references. These amendments are supported throughout the description and drawings, for example, by FIG. 1 of the present application. Applicant respectfully submits that amended claims 1, 21 and 32 are patentable over the cited references for at least the following reasons.

Claims 1, 21, and 32 recite, in part, that "a portion of the gate electrode is embedded in the semiconductor substrate and another portion of the gate electrode is above the semiconductor substrate." Applicant respectfully submits that the cited references fail to teach or suggest this recitation. For example, as shown in FIG. 5(k) of Gardner, the entire gate electrode 530 is disposed between the heavily doped source region 508A and the heavily doped drain region 508B. Clearly, no portion of the gate electrode 530 is "embedded in the semiconductor substrate," as required by claim 1. Moreover, even assuming arguendo that the Examiner characterized the gate electrode 530 as being "embedded" in a substrate, then clearly the gate

electrode 530 would not include a portion "above the semiconductor substrate," as required by the claims. Thus, the cited references fail to teach or suggest that "a portion of the gate electrode is embedded in the semiconductor substrate and another portion of the gate electrode is above the semiconductor substrate," as required by claims 1, 21, and 32. Accordingly, for at least this reason, the rejections under 35 U.S.C. 102(b) and 103(a) should be withdrawn.

The cited references also fail to teach or suggest other features of independent claims 1 and 32.

For example, with respect to claim 1, Applicant respectfully submits that the cited references fail to teach or suggest "a third impurity diffusion layer formed in a portion immediately below the gate electrode in the semiconductor substrate," as required by claim 1. Applicant submits that the doped layer 552 shown in the intermediate structure in FIG. 5E of Gardner et al. does not exist in the IGFET shown in FIG. 5K of Gardner et al. The intermediate structure shown in FIG. 5E of Gardner is not a semiconductor device, and it is the structure shown in FIG. 5K of Gardner et al. is cited by the Examiner in rejecting claim 1. As noted at col. 13, lines 41-50 and as shown in FIG. 5G of Gardner et al., ion implantation (see arrows 520) counterdopes the doped layer 552 effectively splitting doped layer 552 into lightly doped source and drain regions 552A and 552B. Applicant thus submits that the doped layer 552 is not present once counterdoping takes place. Therefore, Gardner et al. does not teach or suggest a semiconductor device that includes an "impurity diffusion layer ... immediately below the gate electrode," as required by claim 1. For at least this additional reason, Applicant submits that claim 1 is patentable over the cited references.

With respect to claim 32, for example, Applicant respectfully submits that the cited references fail to teach or suggest that "a width of the upper surface of the gate electrode substantially equals the width of the groove," as required by claim 32. Applicant submits that FIG. 5K of Gardner clearly illustrates that the oxide spacers 522A,B are disposed between the upper surface of the gate electrode 530 and the sidewalls 516A,B. Thus, the width of the upper surface of the gate electrode 530 does not substantially equal the trench 514, as required by claim 32.

For at least the foregoing reasons, Applicant submits that independent claims 1, 21 and 32 are patentable over the cited references. Dependent claims 2-4, 7, 9, 11, and 33-36; 22-24,

28-29, 31, and 37-40; and 41-43 are also patentable at least by virtue of their dependency from claims 1, 21 and 32, respectively.

Applicant also submits that many of the dependent claims are separately patentable.

Claims 2 and 22

For example, claims 2 and 22 require that "a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric layer is between about 0.05 and 0.15 μm ." In rejecting claim 2, the Examiner reasons that Gardner discloses this feature at column 3, line 10. Applicant respectfully submits that the cited portion of the Gardner patent discusses channel length, and not a distance between "the surface of the first and second impurity diffusion layers" and "the interface between the semiconductor substrate and the gate dielectric layer is between about 0.05 and 0.15 μm ," as recited in claims 2 and 22. Accordingly, the rejections of claims 2 and 22 should be withdrawn.

Claims 4 and 24

Claims 4 and 24 require that "the gate electrode is formed from at least one alloy that includes at least two constituents selected from the following group: polycrystalline silicon, tungsten, tantalum, copper and gold." In rejecting claim 4, the Examiner alleges that Gardner discloses this feature at column 13, line 66 – column 14, line 61. Applicant respectfully submits that of the five alternatives required by claims 4 and 24, the cited portion of the Gardner patent discloses only tungsten. Accordingly, the Gardner patent does not teach or suggest that "the gate electrode is formed from at least one alloy that includes at least two constituents selected from the following group: polycrystalline silicon, tungsten, tantalum, copper and gold," as required by claim 4. Accordingly, the rejections of claims 4 and 24 should be withdrawn.

Claims 7 and 28

Claim 7 requires that "the first and second impurity diffusion layers include an extension region." Claim 28 recites "a third impurity diffusion layer immediately below the gate electrode in the semiconductor substrate, wherein the third impurity diffusion layer is of the opposite conductivity type as the semiconductor substrate, and wherein the first and second impurity diffusion layers include an extension region." In rejecting claim 7, the Examiner reasons that FIG. 5K of Gardner includes "an extension 552A/552B". However, in rejecting claim 1, the Examiner also takes the inconsistent position that the N-doped layer 552 is "a third impurity diffusion layer." Applicant respectfully submits that it is improper to characterize the N-doped

layer 552, which later becomes the lightly doped source and drain regions 552A,B via counterdoping, as meeting both the "third impurity diffusion layer" and the "extension region" limitations of claim 7. In addition, Applicant also submits that the N-doped layer 552 is not present once counterdoping takes place. For this additional reason, the rejection of claims 7 and 28 should be withdrawn.

New dependent claims 33-43

The new dependent claims are also separately patentable over the cited references since the references fail to teach or suggest recitations of those claims, such as, that "the gate electrode is partially interposed between the first and second impurity diffusion layers," that "at least another portion of the gate electrode is above the semiconductor substrate, and the first and second impurity diffusion layers," that "the third impurity diffusion layer is completely disposed between the first and second impurity diffusion layers," and that "the extension regions of the first and second impurity diffusion layers are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions." Thus, Applicant submits that the newly added dependent claims are also patentable over the cited references.

Applicant believes the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6793 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Date: February 13, 2003

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FEB 13 2003

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Version with markings to show changes made:

IN THE CLAIMS:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer formed on the indented section;

a gate electrode formed on the [semiconductor substrate through a] gate dielectric layer,
wherein a portion of the gate electrode is embedded in the semiconductor substrate and another
portion of the gate electrode is above the semiconductor substrate;

first and second impurity diffusion layers formed in the semiconductor substrate and
opposed to each other with the gate electrode being interposed between them;

a third impurity diffusion layer formed in a portion immediately below the gate electrode
in the semiconductor substrate; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof
toward an upper surface thereof, and

wherein surfaces of the first and second impurity diffusion layers are located at a position
higher than an interface between the semiconductor substrate and the gate dielectric layer.

Please cancel claims 5, 6, 10, and 12-20 without prejudice.

21. (Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer formed on the indented section;

a gate electrode formed on the [semiconductor substrate through a] gate dielectric layer,
wherein a portion of the gate electrode is embedded in the semiconductor substrate and another
portion of the gate electrode is above the semiconductor substrate;

first and second impurity diffusion layers formed in the semiconductor substrate and
opposed to each other with the gate electrode being interposed between them; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof,

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, and

wherein surfaces of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region.

Please cancel claims 25-27 and 30 without prejudice or disclaimer.

28. (Amended) A semiconductor device according to claim 21, further comprising:

[wherein] a third impurity diffusion layer [is formed in a portion] immediately below the gate electrode in the semiconductor substrate, wherein the third impurity diffusion layer is of the opposite conductivity type as the semiconductor substrate, and wherein the first and second impurity diffusion layers include an extension region.

32. (Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer formed on the indented section;

a groove section formed at a specified location in the semiconductor substrate;

a gate electrode formed on [a bottom surface of the groove section through a] the gate dielectric layer, wherein a portion of the gate electrode is embedded in the semiconductor substrate and another portion of the gate electrode is above the semiconductor substrate,[:]

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and a width of the upper surface of the gate electrode substantially equals [to a] the width of the groove.